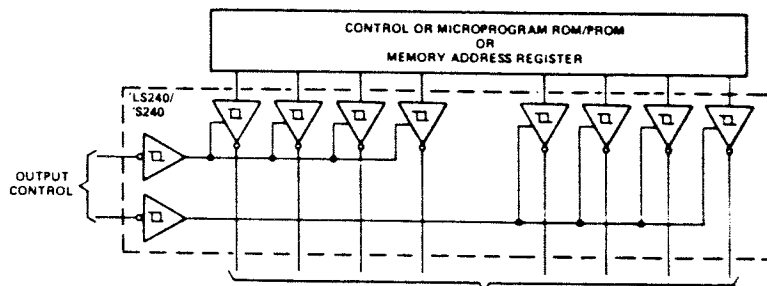
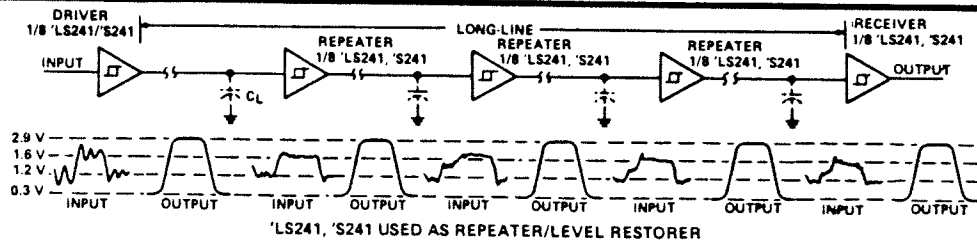
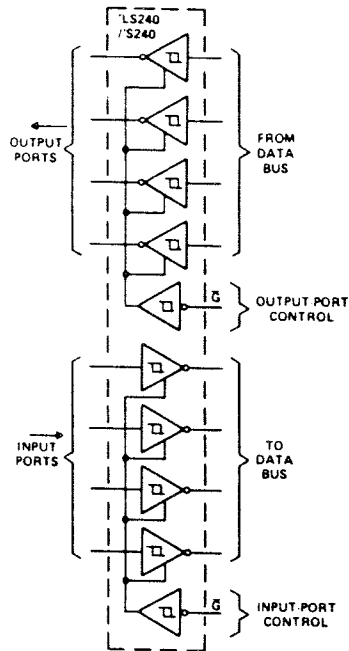


**TYPES SN54LS240, SN54LS241,
SN54LS244, SN54S240, SN54S241, SN74LS240,
SN74LS241, SN74LS244, SN74S240, SN74S241**
OCTAL BUFFERS AND LINE DRIVERS WITH 3-STATE OUTPUTS

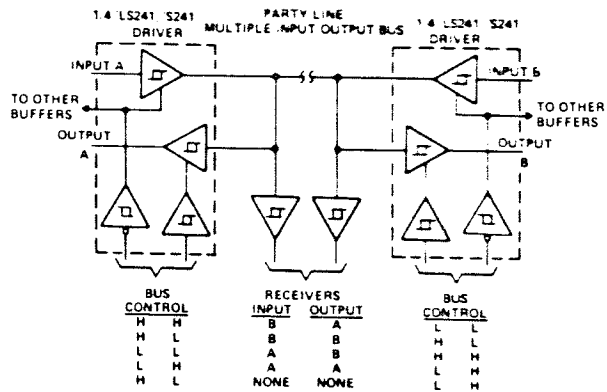


'LS241,'S240 USED AS SYSTEM AND/OR MEMORY BUS DRIVER—4-BIT ORGANIZATION CAN BE APPLIED TO HANDLE BINARY OR BCD

6



INDEPENDENT 4-BIT BUS DRIVERS/RECEIVERS IN A SINGLE PACKAGE



PARTY-LINE BUS SYSTEM WITH MULTIPLE INPUTS, OUTPUTS, AND RECEIVERS
External resistance between any input of the 'S240 or 'S241 and ground or V_{CC} must not exceed 40 k Ω .

POSITIVE-NOR GATES WITH TOTEM-POLE OUTPUTS

recommended operating conditions

PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54				SERIES 54L				SERIES 54LS				SERIES 54S					
			SERIES 74		SERIES 74L		SERIES 74		SERIES 74L		SERIES 74LS		SERIES 74LS		SERIES 74S		SERIES 74S			
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
Supply voltage, V _{CC}			4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5
High-level output current, I _{OH}			4	7.5	5	5.25	4	7.5	5	5.25	4	7.5	5	5.25	4	7.5	5	5.25	4	7.5
Low-level output current, I _{OL}			16			16			2			2			4			8		
Operating free-air temperature, T _A			0	70	0	70	0	70	0	70	0	70	0	70	0	70	0	70	0	70

electrical characteristics over recommended operating free air temperature range (unless otherwise noted)

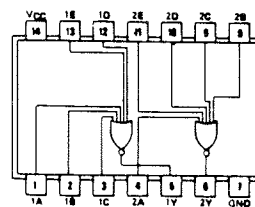
PARAMETER	TEST FIGURE	TEST CONDITIONS†	SERIES 54				SERIES 54L				SERIES 54LS				SERIES 54S					
			SERIES 74		SERIES 74L		SERIES 74		SERIES 74L		SERIES 74LS		SERIES 74LS		SERIES 74S		SERIES 74S			
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
V _{IH} High-level input voltage	1, 2	V _{CC} MIN, I _I = 0	0.8			0.7			0.7			0.7			0.8			0.8		
V _{IL} Low-level input voltage	1, 2	V _{CC} MIN, I _I = 0	0.8			0.7			0.8			0.8			0.8			0.8		
V _{IK} Input clamp voltage	3	V _{CC} MIN, I _I = 0	1.5			1.5			1.5			1.5			1.5			1.5		
V _{OH} High-level output voltage	1	V _{CC} MIN, V _{IL} MAX, I _{OH} MAX	2.4	3.4	7.4	3.3	7.4	3.2	2.5	3.4	7.4	3.4	7.4	3.4	2.5	3.4	7.4	3.4	7.4	3.4
V _{OL} Low-level output voltage	2	V _{CC} MIN, I _{OL} MAX, V _{IH} = 2 V	0.2	0.4	0.2	0.4	0.2	0.4	0.25	0.4	0.25	0.4	0.25	0.4	0.25	0.4	0.25	0.4	0.25	0.4
I _I Input current at maximum input voltage	4	V _{CC} = MAX	1			1			0.1			0.1			1			1		
I _{IH} High-level input current	4	V _{CC} = MAX	40			40			10			10			40			40		
I _{IL} Low-level input current	4	V _{CC} = MAX	160			160			20			20			160			160		
I _{OS} Short-circuit output current*	5	V _{CC} - MAX	-1.6			-1.6			-0.18			-0.18			-1.6			-1.6		
I _{CC} Supply current	7	V _{CC} - MAX	-6.4			-6.4			-2			-2			-6.4			-6.4		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ I_I = -12 mA for SN54/SN74* and 18 mA for SN54LS/SN74LS* and SN54S/SN74S*.

¶ Not more than one output should be shorted at a time, and for SN54LS/SN74LS* and SN54S/SN74S*, duration of output short-circuit should not exceed one second.



POSITIVE-NOR GATES WITH TOTEM-POLE OUTPUTS

supply current[†]

TYPE	I _{CCH} (mA) Total with outputs high		I _{CCL} (mA) Total with outputs low		I _{CC} (mA) Average per gate (50% duty cycle)	
	TYP	MAX	TYP	MAX	TYP	MAX
'02	8	16	14	27	2.75	
'25	8	16	10	19	2.25	
'27	10	16	16	26	4.34	
'L02	0.8	1.6	1.4	2.6	0.275	
'LS02	1.6	3.2	2.8	5.4	0.55	
'LS27	2.0	4	3.4	6.8	0.9	
'S02	17	29	26	45	5.38	
'S260	17	29	26	45	10.75	

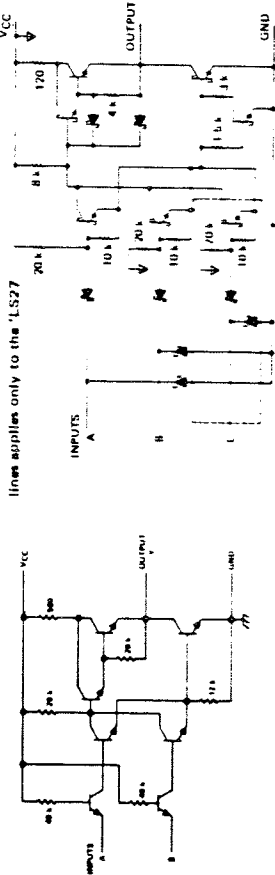
[†]Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A. Typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS [#]	t _{PLH} (ns) Propagation delay time, low-to-high-level output		t _{PHL} (ns) Propagation delay time, high-to-low-level output			
		MIN	TYP	MAX	MIN	TYP	MAX
'02	C _L = 15 pF, R _L = 400 Ω		12	22	8	15	
'25			13	22	8	15	
'27			10	15	7	11	
'L02	C _L = 50 pF, R _L = 4 kΩ		31	60	35	60	
'LS02, 'LS27	C _L = 15 pF, R _L = 2 kΩ		10	16	10	15	
'S02	C _L = 15 pF, R _L = 280 Ω		3.5	5.5	3.5	5.5	
'S260	C _L = 50 pF, R _L = 280 Ω		5	5.5	5	5.5	
	C _L = 15 pF, R _L = 280 Ω		4	5.5	4	6	

[#]Load circuit and voltage waveforms are shown on pages 3-10 and 3-11.

The portion of the schematic within the dashed lines applies only to the 'LS27

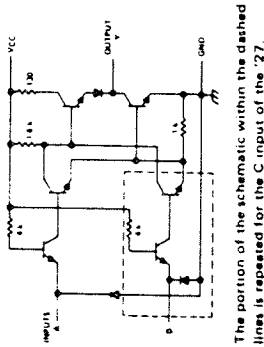


'L02 CIRCUITS

'LS27 CIRCUITS

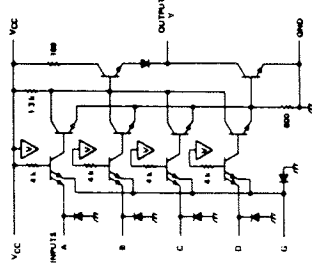
6

schematics (each gate)



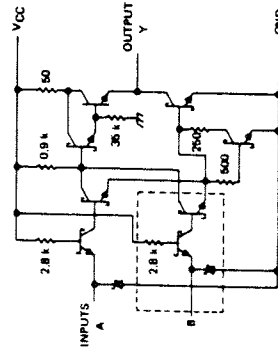
The portion of the schematic within the dashed lines is repeated for the C input of the '27.

'02, '27 CIRCUITS



'25 CIRCUITS

Resistor values are nominal and in ohms.



The portion of the schematic within the dashed lines is repeated for each additional input of the 'S260, and the 0.9 kΩ resistor is changed to 0.6 kΩ.

'S02, 'S260 CIRCUITS

**TTL
MSI**

**TYPES SN54LS266, SN74LS266
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES
WITH OPEN-COLLECTOR OUTPUTS**

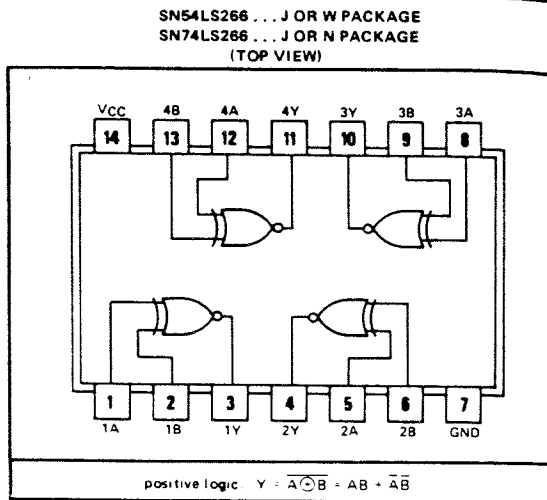
BULLETIN NO. DL-S 7611843, DECEMBER 1972—REVISED OCTOBER 1976

- Can Be Used as a 4-Bit Digital Comparator
- Input Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL and DTL Circuits

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = high level, L = low level

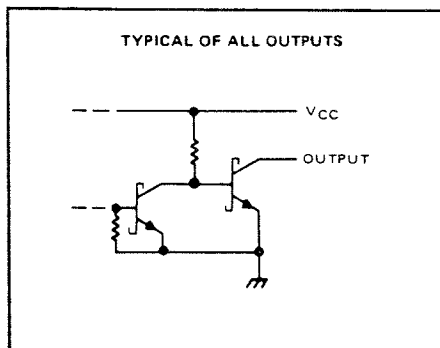
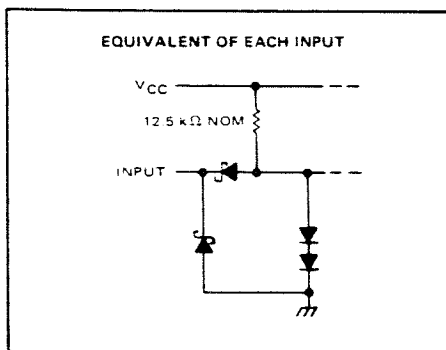


description

The ¹LS266 is comprised of four independent 2-input exclusive-NOR gates with open-collector outputs. The open-collector outputs permit tying outputs together for multiple-bit comparisons.

schematics of inputs and outputs

7



TYPES SN54LS266, SN74LS266 QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

REVISED OCTOBER 1976

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS266	-55°C to 125°C
SN74LS266	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS266			SN74LS266			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS266			SN74LS266			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V_{IH} High-level input voltage		2			2			V	
V_{IL} Low-level input voltage			0.7			0.8		V	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN.}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V	
I_{OH} High-level output current	$V_{CC} = \text{MIN.}$, $V_{IH} = 2 \text{ V.}$ $V_{IL} = V_{IL \text{ max.}}$, $V_{OH} = 5.5 \text{ V}$			100			100	μA	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN.}$, $V_{IH} = 2 \text{ V.}$ $V_{IL} = V_{IL \text{ max.}}$		$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	0.25	0.4	0.25	0.4	V	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX.}$, $V_I = 7 \text{ V}$			0.2			0.2	mA	
I_{IH} High-level input current	$V_{CC} = \text{MAX.}$, $V_I = 2.7 \text{ V}$			40			40	μA	
I_{IL} Low-level input current	$V_{CC} = \text{MAX.}$, $V_I = 0.4 \text{ V}$			-0.8			-0.8	mA	
I_{CC} Supply current	$V_{CC} = \text{MAX.}$, See Note 2			8	13		8	13	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$.

NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ \text{C}$

PARAMETER†	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
		Other input low	Other input high				
t_{PLH}	A or B	Other input low	$C_L = 15 \text{ pF.}$ $R_L = 2 \text{ k}\Omega,$ See Note 3	18	30		ns
t_{PHL}							
t_{PLH}	A or B	Other input high	See Note 3	18	30		ns
t_{PHL}							

† t_{PLH} = propagation delay time, low-to-high-level output

‡ t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuit and voltage waveforms are shown on page 3-11.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

7-387

TTL
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TYPES SN54273, SN54LS273, SN74273, SN74LS273
OCTAL D-TYPE FLIP-FLOP WITH CLEAR

BULLETIN NO. DL S 7612091, OCTOBER 1976

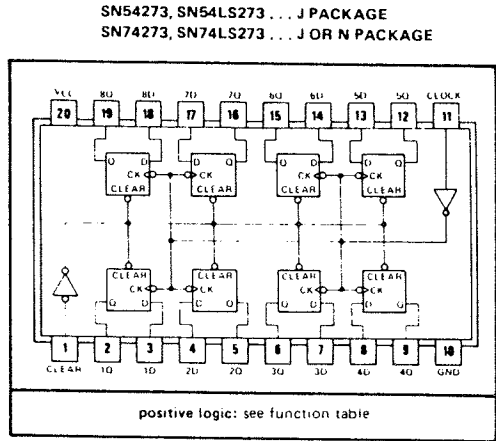
- Contains Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications Include:
 Buffer/Storage Registers
 Shift Registers
 Pattern Generators

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30 megahertz while maximum clock frequency is typically 40 megahertz. Typical power dissipation is 39 milliwatts per flip-flop for the '273 and 10 milliwatts for the 'LS273.

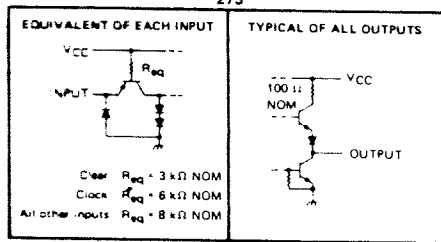


FUNCTION TABLE
(EACH FLIP FLOP)

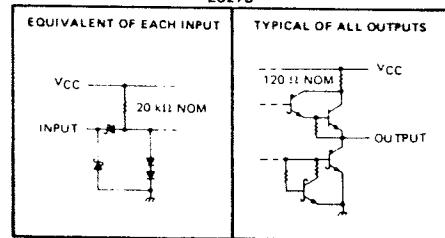
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	'	H	H
H	'	L	L
H	L	X	Q ₀

See explanation of function tables on page 3-8

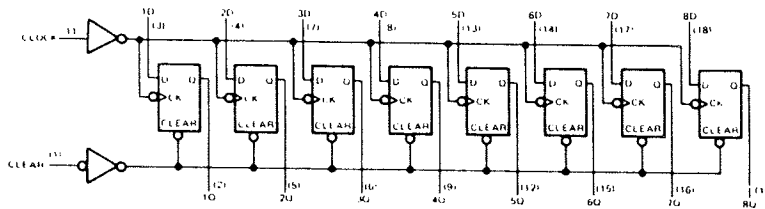
7 schematics of inputs and output
'273



'LS273



functional block diagram



7-388

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

TYPES SN54273, SN74273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54273	-55°C to 125°C
SN74273	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1 Voltage values are with respect to network ground terminal

recommended operating conditions

	SN54273			SN74273			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		30	0		30	MHz
Width of clock or clear pulse, t_w		16.5			16.5		ns
Set-up time, t_{su}	Data input	20†		20†			ns
	Clear inactive state	25†		25†			
Data hold time, t_h		5†		5†			ns
Operating free-air temperature, T_A	-55		125	0		70	C

†The arrow indicates that the rising edge of the clock pulse is used for reference

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage			2		V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$			0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	Clear			80	μ A
	Clock or D	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$		40	
I_{IL} Low-level input current	Clear			-3.2	mA
	Clock or D	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$		-1.6	
I_{OS} Short-circuit output current‡	$V_{CC} = \text{MAX}$	-18		-57	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}$, See Note 2		62	94	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Note 3	30	40		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear		18	27		ns
t_{PLH} Propagation delay time, low-to-high-level output from clock		17	27		ns
t_{PHL} Propagation delay time, high-to-low-level output from clock		18	27		ns

NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54LS273, SN74LS273 OCTAL D-TYPE FLIP-FLOP WITH CLEAR

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS273	-55°C to 125°C
SN74LS273	0°C to 70°C
Storage temperature range	65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

	SN54LS273			SN74LS273			UNIT		
	MIN	NOM	MAX	MIN	NOM	MAX			
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V		
High-level output current, I_{OH}			-400			-400	μ A		
Low-level output current, I_{OL}			4			8	mA		
Clock frequency, f_{clock}	0		30	0		30	MHz		
Width of clock or clear pulse, t_w	20			20			ns		
Set-up time, t_{su}	Data input			20†			ns		
	Clear inactive state			25†					
Data hold time, t_h	5†			5†			ns		
Operating free-air temperature, T_A	-55			125			0	70	°C

†The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS273		SN74LS273		UNIT
		MIN	TYP‡ MAX	MIN	TYP‡ MAX	
V_{IH} High-level input voltage		2		2		V
V_{IL} Low-level input voltage			0.7		0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$		-1.5		-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4	2.7	3.4	V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4	V
	$V_{IL} = V_{IL \text{ max}}, I_{OL} = 8 \text{ mA}$			0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$		0.1		0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$		20		20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = -0.4 \text{ V}$		-0.4		-0.4	mA
I_{OS} Short-circuit output current‡	$V_{CC} = \text{MAX}$	-20	-100	-20	-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	17	27	17	27	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V is applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency		30	40		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Note 4		18	27	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			17	27	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			18	27	ns

NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

INTERFACE CIRCUITS

SERIES 55460/75460 DUAL PERIPHERAL DRIVERS

BULLETIN NO. DL-S 7712425, DECEMBER 1976—REVISED AUGUST 1977

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

performance

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V
- Medium-Speed Switching

ease-of-design

- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL- or DTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Available in Plastic and Ceramic Packages

SUMMARY OF SERIES 55460/75460

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55460	AND [†]	J
SN55461	AND	JG
SN55462	NAND	JG
SN55463	OR	JG
SN55464	NOR	JG
SN75460	AND [†]	J, N
SN75461	AND	JG, P
SN75462	NAND	JG, P
SN75463	OR	JG, P
SN75464	NOR	JG, P

[†]With output transistor base connected externally to output of gate

description

Series 55460/75460 dual peripheral drivers are functionally interchangeable with Series 55450B/75450B and Series 55460/75460 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers. Series 55460 drivers are characterized for operation over the full military temperature range of -55°C to 125°C, Series 75460 drivers are characterized for operation from 0°C to 70°C.

The SN55460 and SN75460 are unique general-purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high-current, high-voltage, n-p-n transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The SN55461/SN75461, SN55462/SN75462, SN55463/SN75463, and SN55464/SN75464 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic) with the output of the gates internally connected to the bases of the n-p-n output transistors.

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SERIES 55460/75460 DUAL PERIPHERAL DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55460	SN55461 SN55462 SN55463 SN55464	SN75460	SN75461 SN75462 SN75463 SN75464	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	5.5	5.5	5.5	V
Interemitter voltage (see Note 2)	5.5	5.5	5.5	5.5	V
V_{CC} -to-substrate voltage	40		40		V
Collector-to-substrate voltage	40		40		V
Collector-base voltage	40		40		V
Collector-emitter voltage (see Note 3)	40		40		V
Collector-emitter voltage (see Note 4)	25		25		V
Emitter-base voltage	5		5		V
Off-state output voltage		35		35	V
Continuous collector or output current (see Note 5)	400	400	400	400	mA
Peak collector or output current ($t_{pw} < 10$ ms, duty cycle $\leq 50\%$, see Note 5)	500	500	500	500	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)	J package	1375	1025		mW
	JG package		1050	825	
	N package		1150		
	P package			1000	
Operating free-air temperature range	-55 to 125	-55 to 125	0 to 70	0 to 70	°C
Storage temperature range	-65 to 150	-65 to 150	-65 to 150	-65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds	J or JG package	300	300	300	°C
Lead temperature 1/16 inch from case for 10 seconds	N or P package	260	260	260	°C

- NOTES
1. Voltage values are with respect to network ground terminal unless otherwise specified.
 2. This is the voltage between two emitters of a multiple-emitter transistor.
 3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω .
 4. This value applies between 0 and 10 mA collector current when the base-emitter diode is open-circuited.
 5. Both halves of these dual circuits may conduct rated current simultaneously, however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.
 6. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 21. In the J and JG packages, SN55460 through SN55464 chips are alloy-mounted; SN75460 through SN75464 chips are glass-mounted.

recommended operating conditions (see Note 7)

	SERIES 55460			SERIES 75460			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	-55		125	0		70	°C

NOTE 7: For SN55460 and SN75460 only, the substrate (pin 8) must always be at the most negative device voltage for proper operation.